What is claimed is:

- 1 1. A computer system comprising:
- a non volatile memory in which is stored a firmware error handling routine for
- 3 handling errors; and
- 4 at least one processor wherein each of the at least one processors detects errors
- 5 and executes the firmware error handling routine on detecting an error to handle the
- 6 error and wherein the firmware error handling routine logs error information to a log.
- 1 2. The computer system of claim 1, wherein the error handling routine collects
- 2 state information, saves the state information to the log, analyzes the error and attempts
- 3 to correct the error.
- 1 3. The computer system of claim 1 wherein the firmware error handling routine
- 2 analyzes the error and determines a severity of the error and handles a plurality of
- 3 detected errors in order of the severity of the error.
- 1 4. The computer system of claim 2 further comprising:
- a system memory in which is stored an operating error handling routine for
- 3 handling errors; and
- 4 wherein the at least one processor executes the operating system error handling
- 5 routine on failure to correct the error by the firmware error handling routine.
- 1 5. The computer system of claim 4, wherein the operating error handling routine
- 2 attempts to correct the error by terminating processes affected by the error.
- 1 6. The computer system of claim 5, wherein the operating error handling routine
- 2 reboots the system on failure to correct the error.

- 1 7. A computer system comprising:
- a non volatile memory in which is stored a processor abstraction layer error
- 3 handling routine and a system abstraction layer error handling routine; and
- 4 a processor coupled to the non volatile memory for executing the processor
- 5 abstraction layer error handling routine and the system abstraction layer error handling
- 6 routine on detecting an error.
- 1 8. The computer system of claim 7 further comprising:
- 2 platform hardware coupled to the processor, wherein the processor detects errors
- 3 in the platform hardware as errors.
- 1 9. The computer system of claim 7, wherein error handling is cooperatively
- 2 performed by the processor, the processor abstraction layer and the system abstraction
- 3 layer.
- 1 10. The computer system of claim 9, wherein the system abstraction layer error
- 2 handling routine analyzes the error and the state information, obtains additional state
- 3 information by utilizing processor abstraction layer procedures, determines a severity of
- 4 the error, creates a log containing the state information, and attempts to correct the error
- 5 on processor abstraction layer being unable to correct the error.
- 1 11. A computer system comprising:
- 2 a plurality of systems comprising:
- a non volatile memory in which is stored a first error handling routine
- 4 and a second error handling routine; and
- 5 a processor coupled to the non volatile memory to execute the first error
- 6 handling routine and the second error handling routine and to generate an error log on
- 7 detecting an error.

- 1 12. A system for cooperative error handling comprising:
- a memory in which is stored a first error handling routine for correcting errors
- 3 and a second error handling routine for correcting errors; and
- 4 a detecting processor coupled to the non volatile memory to detect errors, to
- 5 execute the first error handling routine on detecting an error, to execute the second error
- 6 handling routine on failure of the first error handling routine to correct the error.
- 1 13. The system of claim 12, further comprising a system memory coupled to the
- 2 detecting processor in which is a third error handling routine wherein the detecting
- 3 processor executes the third error handling routine on failure of the first and second
- 4 error handling routines to correct the error.
- 1 14. A system comprising:
- 2 a processor;
- a system memory; and
- 4 a non-volatile memory in which is stored:
- 5 a first error handling routine executed on an error to access state
- 6 information, store the state information to a log and to attempt to correct the.
- 1 15. The system of claim 14, wherein the non-volatile memory further comprises a
- 2 second error handling routine branched to on completion of the first error handling
- 3 routine, wherein the second error handing routine stores a status of the error and the
- 4 state information to the log and attempts to correct the error.
- 1 16. The system of claim 15, wherein the system memory further comprises a third
- 2 error handling routine executed by the processor on failure of the second error handling
- 3 routine to correct the error, wherein the third error routine accesses the log and attempts
- 4 to correct the error by terminating affected processes and wherein the first error
- 5 handling routine is a processor abstraction layer error handling routine, the second error

- 6 handling routine is a system abstraction layer error handling routine and the third error
- 7 handling routine is an operating system error handling routine.
- 1 17. The system of claim 16, wherein the third error handling routine causes the
- 2 system to reboot on failure to correct the error.
- 1 18. A method for cooperative error handling in a computer system comprising:
- 2 detecting an error by a detecting processor;
- 3 executing error handling code of a first layer of software, by the detecting
- 4 processor, to perform the following:
- 5 saving state information;
- 6 attempting to correct the error;
- 7 on failure to correct the error, executing error handling code of a second layer of
- 8 software by the detecting processor to perform the following:
- 9 determining severity of error by analyzing state information and the error
- 10 received from the first layer;
- saving additional state information; and
- halting the computer system if necessary; and
- on failure to correct the error by the second layer of software, executing error
- 14 handling code of an operating system by the detecting processor to perform the
- 15 following:
- 16 checking state information and the error to see if processing can
- 17 continue;

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- 18 halting the computer system if processing unless processing can
- 19 continue; and
- attempting to correct the error.
 - 19. A method for handling errors in a system comprising:
- 2 detecting an error;
- determining if the error is global or local;

- 4 on the error being global, signaling other processors of the error and allowing
- 5 one processor to control error handling;
- 6 determining if the error is unrecoverable;
- on the error being unrecoverable, halting the system;
- 8 correcting the error.
- 1 20. The method of claim 19, further comprising:
- 2 interrupting affected processes; and
- 3 resuming the affected processes after correcting the error.
- 1 21. The method of claim 19, further comprising:
- 2 saving state information; and
- determining a severity of the error.
- 1 22. A method comprising:
- detecting an error;
- sending a signal to a processor abstraction layer, a system abstraction layer, and
- 4 an operating system of the error;
- 5 interrupting processing if necessary;
- 6 attempting to correct the error by the processor abstraction layer and informing
- 7 the system abstraction layer of success or failure in correcting the error;
- 8 upon success by the processor abstraction layer, informing operating system of
- 9 the correction;
- upon failure by the processor abstraction layer, attempting to correct the error by
- the system abstraction layer and informing the operating system of success or failure;
- upon failure by the system abstraction layer, attempting to correct the error by
- 13 the operating system; and
- upon failure by the operating system, initiating a system reboot.

- 1 23. The method of claim 22, further comprising determining a severity of the error
- 2 and halting system on certain errors.
- 1 24. A computer readable medium containing computer instructions for instructing a
- 2 processor to perform a method for cooperatively handling errors comprising:
- 3 attempting to correct an error by a detecting processor;
- 4 on failure, executing firmware code to correct the error; and
- 5 on failure, executing operating system code to correct the error.
- 1 25. The computer readable medium containing computer instructions for instructing
- 2 a processor to perform a method for cooperatively handling errors, further comprising:
- on the operating system being a legacy operating system, sending compatible
- 4 instructions to the operating system.